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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,834	03/30/2004	Hongjiang Song	884.C61US1	3113

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EXAMINER	
DAGLAWI, AMAR A	

ART UNIT	PAPER NUMBER
2618	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,834	SONG, HONGJIANG	
	Examiner	Art Unit	
	Amar Daglawi	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13,14,16-24 and 27-31* is/are rejected.

7)☒ Claim(s) *12,15,25,26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-7, 9, 11, 13, 14, 22-24, 27-29, 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Luz et al (US 6,321,073 B1).

With respect to claim 1, Luz teaches an apparatus (Fig.3b) comprising:

A comparison unit coupled to an output of a final stage of multiple stages in a receiver channel (Fig.1, Fig.3b, 376, 104a, 104b, 104n, col.5, lines 1-38)

A controller (108) coupled to the comparison unit to calibrate each of the multiple stages (Fig.1, Fig3b, 108, col.4, lines 45-67, col.5, lines 1-36, col.1, lines 58-67).

With respect to claim 2, Luz further teaches the comparison unit includes a single comparator coupled to the output of the final stage, the output to provide a signal representative of a received signal at an input to the receiver channel (Fig.1, col.2, lines 40-62, Fig.3B, col.5, lines 6-25).

With respect to claim 4, Luz further teaches the controller is reconfigurable to test the receiver channel (col.4, lines 45-67).

With respect to claim 5, Luz further teaches the apparatus is a portable wireless receiver (Abstract).

With respect to claim 6, Luz teaches an apparatus (Fig.1, Fig.3B) comprising:

Multiple calibration circuits (106 and 104a and 104b) to calibrate multiple stages in a receiver channel (Fig.1, Fig.3B, col.2, lines 40-67, col.4, lines 45-67, col.3, lines 20-25). A controller coupled to an output of a final stage of multiple stages, the controller to control each of the multiple calibration circuits (Fig.1, Fig.3B, col.4, lines 45-67, col.5, lines 1-30).

With respect to claim 7, Luz further teaches the controller includes a single comparator coupled to the output of the final stage, the final stage output to provide a signal representative of a received signal at an input to the receiver channel (Fig.1, col.2, lines 40-62, Fig.3B, col.5, lines 6-25).

With respect to claim 9, Luz further teaches each calibration circuit is adapted to provide a DC offset calibration (Abstract, col.5, lines 5-30).

With respect to claim 11, Luz further teaches the controller includes a stage selection circuit sequentially calibrate each stage of he multiple stages (Fig.1, 200) wherein each of the calibration circuits is assigned to a separate one of multiple stages (Fig.1, Fig.3B, col.4, lines 45-67, col.5, lines 1-30).

With respect to claim 13, Luz further teaches the comparison unit is adapted compare differential intermediate versions of the received signal (col.4, lines 45-67).

With respect to claim 14, Luz further teaches the controller is reconfigurable to test the receiver channel (col.4, lines 45-67).

With respect to claim 22, Luz teaches a method comprising:

Evaluating a received signal from an output of a final stage of multiple stages in a receiver channel using a single comparison unit (Fig.1, Fig.3b, 376, 104a, 104b, 104n, col.4, lines 45-67,col.5, lines 1-38)

Selectively controlling the calibration of each stage of the multiple stages based on an output from the single comparison unit (Fig.1, Fig3b, 108, col.4, lines 45-67, col.5, lines 1-36, col.1, lines 58-67)

With respect to claim 23, Luz further teaches using a single comparison unit includes using a single comparator (Fig.3B, 376, col.5, lines 5-22).

With respect to claim 24, Luz further teaches selectively controlling the calibration of the multiple stages includes reducing a DC offset to less than 0.5 mV for each stage (col.3, lines 6-20) [It is inherently taught that the Dc off set is less than 0.5 mV for each stage to enable the operational amplifier to be active and to float].

With respect to claim 27, Luz further teaches selectively control the calibration of the multiple stages includes reconfiguring a controller having the single comparator as an input component to test the receiver channel (Fig.1, Fig.3B, col.4, lines 45-67, col.5, lines 1-30).

With respect to claim 28, Luz further teaches the method further includes using the controller to generate a linear ramp signal to test the receiver channel (Fig.4b, col.5, lines 34-60).

With respect to claim 29, Luz teaches a computer-readable medium having computer-executable instructions for performing a method comprising:

Controlling operational modes of controller coupled to an output of a final stage of multiple stages in a receiver channel, wherein one operational mode includes calibrating each stage of the multiple stages based on evaluating a received signal from the final stage using a single comparison unit (Fig.1, Fig.3B, 108 (controller), 376 (comparator), col.4, lines 45-67, col.5, lines 1-38, operational modes include calibration mode and use mode)

With respect to claim 31, Luz further teaches controlling operational modes includes providing a test enable signal to configure the controller to test the receiver channel (col.4, lines 45-67).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3 and 10 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luz et al (US 6,321,073 B1) in view of Walker et al (US 2005/0208919 A1).

With respect to claims 3 and 10 and 31, Luz teaches all the limitations of claims 1 and 6 except for the controller is adapted to decouple from the receiver channel to characterize performance of the receiver channel and the multiple calibration circuits and controller are adapted to decouple from the receiver channel and the controlling operational modes includes providing a selection bypass signal to decouple the controller from the receiver channel and providing instructions to characterize a performance of the receiver channel with the controller decoupled from the receiver channel.

In related art Walker teaches a direct down conversion receiver architecture having a DC loop to remove DC offset from the signal components (Fig.1) where DC offset canceller is decoupled from the signal gain scaling by the DVGA (Fig.1, par [0064]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings of Luz with decoupling the DC offset canceller as taught by Walker so as to adjust the gain on all of the plurality of gain stages based on the required gain for the input signal when the DC offset canceller and controller are decoupled from the receiver.

Claims 16-18, 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luz et al (US 6,321,073 B1) in view of Anderson et al (US 6,876,859 B2).

Luz teaches a receiver channel having multiple stages to convert the signal (Fig.1, Fig.3B, col.2, lines 40-62)

multiple calibration circuits to provide calibration to the multiple stages (Fig.3B, Fig.1, col.4, lines 45-67, col.5, lines 1-30); and

a controller coupled to an output of a final stage of the multiple stages, the controller to control each of the multiple calibration circuits (Fig.1, Fig.3B, col.4, lines 45-67, col.5, lines 1-30).

However, Luz fails to teach a substantially omni-directional antenna to receive a signal and a bandpass filter coupled to the antenna.

In the same field of endeavor Anderson teaches in (Fig.2B, col.10, lines 45-68, col.11, lines 1-21) a band-pass filter and an omni-directional antenna to receive a signal and remove interfering signals from outside the RF band of interest.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings of Luz with the bandpass filter and the omni-directional antenna so as to receive a signal and filter interfering signals from outside the RF band of interest.

With respect to claim 17, Luz further teaches the controller includes a single comparator coupled to the final stage of the multiple stages in the receiver channel (Fig.1, col.2, lines 40-62, Fig.3B, col.5, lines 6-25).

With respect to claim 18, Luz further teaches the controller includes a stage selection circuit to sequentially calibrate each stage in the multiple stages (Fig.1, 200) wherein each of the calibration circuits is assigned to a separate one of multiple stages (Fig.1, Fig.3B, col.4, lines 45-67, col.5, lines 1-30).

With respect to claim 20, Luz further teaches the controller is reconfigurable to test the receiver channel (col.4, lines 45-67).

With respect to claim 21, Luz further teaches the system is a portable wireless communication system (Abstract).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Luz (6,321,073) in view of Anderson (US 6,876,859 as applied to claim 16 above, and further in view of Walker et al (US 2005/0208919 A1).

Luz in view of Anderson teach all the limitations of claim 16 except for the multiple calibration circuits and the controller are adapted to decouple from the receiver.

In related art Walker teaches a direct down conversion receiver architecture having a DC loop to remove DC offset from the signal components (Fig.1) where DC offset canceller is decoupled from the signal gain scaling by the DVGA (Fig.1, par [0064]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings of Luz with decoupling the DC offset canceller as taught by Walker so as to adjust the gain on all of the plurality of gain

stages based on the required gain for the input signal when the DC offset canceller and controller are decoupled from the receiver.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Luz et al (US 6,321,073) in view of Oono et al (US 2002/0094792 A1).

Luz teaches all the limitations of claim 7 except for each calibration circuit is assigned to one stage of the multiple stages the multiple stages being a sequence of filter stages in the receiver.

Oono teaches a sequence of filter stages and an auto calibration circuit which effects DC offset calibration (Fig.4, par [0038]).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings of Luz with the sequence of filters so as to achieve a DC offset calibration for each filter with the calibration circuit.

Allowable Subject Matter

Claims 12, 15, 25 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: The primary reason for indication of allowability:

With respect to claim 12, the prior art does not teach or fairly suggest in combination with the other claimed limitation a comparison unit coupled to the final stage to evaluate a received signal propagating through the receiver channel;
multiple registers coupled to the stage selection circuit, each register associated with a separate one of the multiple stages, each register to hold a signal to provide DC offset calibration to its associated stage; and
a modulator to provide each register with its signal to provide DC offset calibration to its associated stage, the modulator responsive to an output of the comparison unit.

With respect to claim 15, the prior art does not teach or fairly suggest in combination a stage selection circuit to select one or more of the multiple stages to receive a test signal;
multiple registers, each register associated with a separate one of the multiple stages to provide its associated stage with its test signal, each register responsive to the stage selection circuit;
a modulator having a test enable input and test signal circuits to provide each register with its test signal.

With respect to claim 25, the prior art does not teach or fairly suggest in combination selectively controlling the calibration of the multiple stages includes decoupling a controller having the single comparison unit as an input component from the receiver channel and decoupling calibration circuits that are adapted to calibrate the multiple stages from the receiver channel.

With respect to claim 26, is objected for being dependent on another objected claim.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amar Daglawi whose telephone number is 571-270-1221. The examiner can normally be reached on Monday- Friday (7:30 AM- 5:00 AM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571-272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amar Daglawi

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